

## CLAIMS

1. A light-emitting thyristor matrix array formed on a chip comprising :

5 N (N is an integer  $\geq 2$ ) three-terminal light-emitting thyristors arrayed in one line in parallel with the long side of the chip ; and

a plurality of bonding pads arrayed in one line in parallel with the long side of the chip.

10 2. The light-emitting thyristor matrix array of claim 1, further comprising :

a common terminal to which cathodes or anodes of the N light-emitting thyristors are connected ; and

M (M is an integer  $\geq 2$ ) gate-selecting lines ;

15 wherein the gate of kth light-emitting thyristor is connected to ith [ $i = \{(k-1) \text{ MOD } M\} + 1$ ] gate-selecting line  $G_i$ ,

the anode or cathode which is not connected to the common terminal of the kth light-emitting thyristor is connected to jth [ $j = \{(k-i)/M\} + 1$ ] anode terminal  $A_j$  or  
20 cathode terminal  $K_j$ .

3. The light-emitting thyristor matrix array of claim 2, wherein the number M of the gate-selecting lines satisfies the relationship of  $L/\{(N/M)+M\} > p$  (L is a length of the long  
25 side of the chip and p is a critical value of the array pitch of the bonding pads).

4. The light-emitting thyristor matrix array of claim 3, wherein the critical value p of the array pitch of the  
30 bonding pads is about  $75 \mu\text{m}$ .

5. The light-emitting thyristor matrix array of claim 3, wherein when a prime factor for N is 2 only, the number M of the gate-selecting lines is the smallest integer, next smaller integer, or third smaller integer.

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6. The light-emitting thyristor matrix array of claim 3, wherein when prime factors for N are 2 and 3 only, the number M of the gate-selecting lines is the smallest integer, next smaller integer, third smaller integer, fourth smaller integer, or fifth smaller integer.

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7. The light-emitting thyristor matrix array of claim 1, further comprising :

a common terminal to which cathodes or anodes of the N light-emitting thyristors are connected ; and

M (M is an integer  $\geq 2$ ) anode-selecting lines or cathode-selecting lines ;

wherein the anode or cathode of kth light-emitting thyristor is connected to ith  $[i = \{(k-1) \text{ MOD } M\} + 1]$  anode-selecting line  $A_i$  or cathode-selecting line  $K_i$ ,

the gate of the kth light-emitting thyristor is connected to jth  $[j = \{(k-i)/M\} + 1]$  gate terminal  $G_j$ .

8. The light-emitting thyristor matrix array of claim 7, wherein the number M of the anode-selecting lines or cathode-selecting lines satisfies the relationship of  $L/\{(N/M)+M\} > p$  (L is a length of the long side of the chip and p is a critical value of the array pitch of the bonding pads).

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9. The light-emitting thyristor matrix array of claim 8,

wherein the critical value  $p$  of the array pitch of the bonding pads is about  $75\mu\text{m}$ .

10 11. The light-emitting thyristor matrix array of claim 8,  
5 wherein when a prime factor for  $N$  is 2 only, the number  $M$  of the anode-selecting lines or cathode-selecting lines is the smallest integer, next smaller integer, or third smaller integer.

10 12. The light-emitting thyristor matrix array of claim 8,  
wherein when prime factors for  $N$  are 2 and 3 only, the number  $M$  of the anode-selecting lines or cathode-selecting lines is the smallest integer, next smaller integer, third smaller integer, fourth smaller integer, or fifth smaller integer.

15 13. A driver circuit for driving the light-emitting thyristor matrix array according to any one of claims 2-6, comprising :  
a circuit for driving the gate-selecting lines ; and  
a circuit for driving the anode terminals or cathodes  
20 terminal ;

wherein the circuit for driving the gate-selecting lines including even number of gate-selecting signal output terminals and a circuit for outputting a "selecting" signal to one of the gate-selecting signal output terminals and "no-selecting" signal to the others of the gate-selecting signal  
25 output terminal, with the terminal to which the "selecting" signal is supplied being switched in turn.

13. The driver circuit of claim 12, wherein a serial  
30 input/parallel output shift register is used for the circuit

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14. The driver circuit of claim 13, wherein the number of the gate-selecting signal output signal terminals is any one of 4, 5 6, 8, 12 and 16.